REMARKS

We are in receipt of the Office Action dated January 4, 2005, and the following remarks are made in light thereof.

Claims 1-36 are pending in the application, with claims 1-10 having been withdrawn from consideration. Pursuant to the Office Action, claims 11-18, 23-32 and 34-35 are rejected for being anticipated by Kern, "Handbook of Semiconductor Wafer Cleaning Technology." Claims 19-22 and 36 are rejected for anticipation by Chiyou et al., Patent Abstracts of Japan 11-016866.

Turning first to the rejection over Kern, the Examiner asserts that Kern teaches forming a semiconductor. However, Kern only uses the term "device surface" (see page 3, line 6).

In addition, the Examiner takes the position that Kern teaches fabricating a DRAM device of ULSI silicon circuits; that it is well known that DRAM devices require gate insulators as part of the fabrication scheme; and that since Kern teaches the fabrication of various semiconductor devices, the wiring layer is inherent. Based upon this view, the Examiner concludes that Kern teaches (1) forming a gate insulating film in contact with the semiconductor film having a surface from which the contaminating impurity has been removed (claims 11 and 15); (2) forming a gate wiring over a substrate; and (3) forming a gate insulating film and a semiconductor film over the gate wiring after the contaminating impurities are removed from the surface (claims 23 and 27). However, there is no clear teaching in Kern of steps (1)-(3).

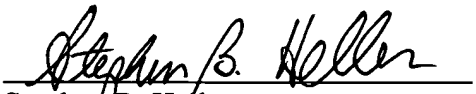
The Examiner also asserts that Kern teaches forming at least one semiconductor island over a substrate, referring to Fig. 29 on page 483. However, the cited figure appears to disclose an adstructure, which is a defect in manufacturing a semiconductor device that should be removed before forming a gate insulating film.

Accordingly, Applicant submits that Kern does not teach forming a semiconductor island over a substrate, and that this rejection should be withdrawn.

Turning to the rejection over Chiyou et al., the Examiner asserts that Chiyou et al. teach forming at least one semiconductor island over a substrate by patterning the crystallized semiconductor film, referring to Drawing 3. However, Drawing 3A denotes a water drop on a silicon surface, and Drawing 3B denotes silicon oxide (i.e., a water mark) on a silicon surface. However, Chiyou et al. fail to teach the claim step of "forming a gate insulating film over said semiconductor island." Accordingly, Applicant submits that Chiyou et al. does not anticipate the rejected claims.

Based upon the foregoing, Applicant submits that the pending claims cannot be rejected for anticipation by either Kern or Chiyou et al. and that this rejection be withdrawn and the claims allowed.

Respectfully submitted,



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